Systel™ IDC2000 - A Novel Digital Configurable Power Management SoC Controller for Lighting and Building Automation

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Introduction

This paper introduces the IDC2000 (Integrated Digital Control 2000) digital power management SoC (system on chip) controller aimed at the lighting and building automation market. This chip is based on architecture of multiple smart configurable logic engines with embedded Power Line Modem, RF, I^2C and other communication interface implemented in a mixed-signal SoC platform. This platform is designed for the broad power electronics industry and was developed to allow a complete migration path from analog to digital control in applications in which the advantages of the digital technology prevail.

The IDC2000 is a scalable SoC controller platform composed of configurable logic engines - building blocks. The first two chips to be introduced are a 1.8V/3.3V SoC aimed for lighting and building automation. The IDC2000 chips are accompanied by a reference design board and two proprietary design tools; the PDK™ and the PowerScene™.

This SoC controller platform has features like minimal latency influence, fast control, broad bandwidth and high resolution (Table 1) that are normally envisioned as being only provided by analog ASIC solutions. The chip incorporates digital benefits by providing short "time-to-market" by using a no code programming method.

The logic engines are configurable to allow this platform to match most desired power topologies and to implement all the requested control algorithms and operational functions.

This resulting solution achieves optimal performance of the end product. In lighting, for example, this controller allows for dimming and adapting ballast to different types of lamps without changing capacitors, resistors or magnetics.

Functional Partitioning of the IDC2000 Architecture

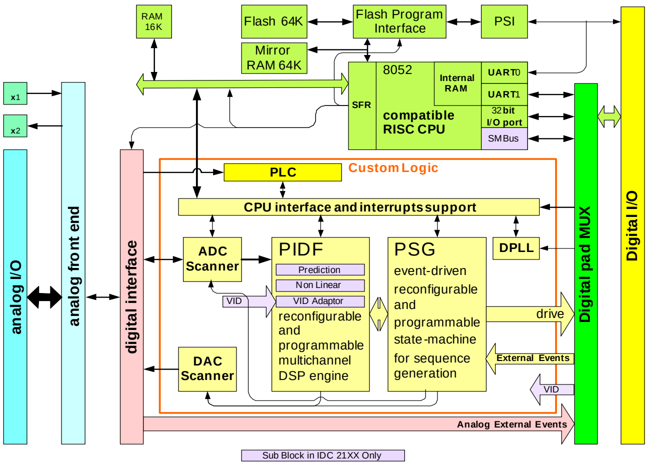
- Single chip solution - All power control and power management and communications in a single SoC
- Configurable architecture
- All measurements and calculation by logic engines - building blocks
- All control loops processed in digital building blocks
- All the power sequential driver signals are generated by building blocks
- All power switches and drivers are outside the SoC
- Differential analog section for high noise immunity
- Multipurpose Digital I/O

Table 1 IDC2000 Main Outstanding Characteristics

Function	IDC2000 - 108L
PSG Clock Frequency	192MHz
PSG switching signal resolution	5.3nS
Average PSG signal resolution by dithering	0.17nS
PSG pulse duration– Max # of bits	12
Minimum Pulse Width	26.5nS
Maximum Pulse Width	22.2mS
Minimum Control Calculation Updating Time	500nS
Control Functions	By PIDF logic engines
Minimum Total Control Latency	700nS
PSG - # of states per cycle	Configurable, up to 16 states
PSG /modulation control method	Flexible Sequence - PWM, FM, or any combination
PSG pulse sequence structure	Configurable On-the-Fly
PSG pulse sequence	Responding to external and/ or internal events
Number of PSGs outputs	11 + 11 complementary PSG outputs or software controlled
Number of analog inputs	24+ 3 internal (for temp. and VDD measurement)
Digital I/O	52 (10 schmidt-trigger inputs)
Analog input resolution	10Bit
Analog input sample - effective rate	up to 12MHz flexible sharing its time resources between inputs by priorities
PSG frequency	1500kHz/12 Bit
	3000kHz/11 Bit
Current Mode Control	Yes
Power Factor Correction	Configurable

Abbreviations appearing in this article
PSG – Pulse Sequence Generator Output Drive Signals
I/O - input/output
PIDF- Proportional/Integral/Differential/Feed-forward
SPI – programming serial interface
DPLL – digital phase lock loop
GUI – Graphical User Interface

Figure 1 IDC2000 Block Diagram



IDC2000 Architecture Structure Explanation

The IDC2000-108L, the full-function version for lighting applications, has 11 closed loop control and signal generators for creating 11 switching sequential drive signals or signal pairs. Each of the channels comprises over 50 configurable parameters. This ASIC is designed for regular and networkable multi-fixture ballasts and multi-lamp ballasts of 8 lamps with emergency feature The second chip version, the IDC2000-64L comprises 6 signal generators and is targeted for regular or networkable ballasts of up to 4 lamps.

The IDC2000 architecture is composed of configurable logic engines - Building Blocks as mentioned above and can be configured and interconnected according to designer needs to create his own solution.

The IDC2000 building blocks are described as follows (and for the sake of brevity only some essential configurable parameters are referred to).

IDC CPU

The CPU is involved in relatively slow and/or sophisticated control closed loop. Its main task is to wake up the SOC by loading the application configuration from flash or ROM into the Custom Logic and support the communication interfaces including the PLC (power line carrier) modem logic block.

Most of the Custom Logic configurable parameters can be modified (updated) during operation (on-the-fly) in order to adapt to changes in the operating conditions (load change, supplied voltages change, etc.).

The Custom Logic controls all the required building blocks for closing the control loop and the generation of driving signals required by almost any known switching power machine. Each building block has configurable parameters for adapting its behavior to the implemented application.

Analog Front-End

Includes the following elements and their functions:
ADC/DAC – generates analog reference to analog comparators,
Track and Hold (T&H) – enable sampling of analog input at certain timing in relation to switching drive signals,
Invert Amplifier – allows sampling of negative signal,
Variable Gain Amplifier – keeps high resolution for small signal,
Differential Amplifier – for achieving high noise immunity, Analog Comparators – for creating events used in generation of some drive signals, for example current mode control.

The ADC and associate elements are commanded by the ADC Scanner (via digital interface) for the sampling rate and sequence of the analog inputs i.e. feedback signals, voltages, currents, temperatures etc. and converting them to digital data by the ADC. The ADC Scanner includes Digital Filter for noise rejection, RAM for all inputs converted data (each input has its own address) used for filtering operation and enabling software monitoring. The data in the RAM is updated whenever the related analog input is sampled.

The DAC and its associate elements are commanded by the DAC Scanner mainly for creating the required references to the analog comparators.

PIDF Building Block

The PIDF module includes 6 or 11 identical channels. Each channel is a digital configurable close loop control logic engine to stabilize the application output parameters. Each channel is able to support one or more PSG channel. In addition, to the proportional, integral and differential functions the engine also provides a feed-forward function for superior loop contr5ol and stability.

PSG Building Block

The PSG Module includes 6 or 11 identical channels. Each channel is a configurable event driven periodic state machine comprising 16 states. Each channel has 2 outputs: PSG output for signal programmed in its LUT and SPWM (software pulse width modulation) Output for software controlled PWM. The SPWM Output also serves as a complementary output (with programmed Dead Time) to PSG Signal when the Complementary Mode is selected (for Half Bridge like drive signals). Each channel has 2 counters of 12 bits, 3 digital comparators, 2 CPU Data Registers, 2 PIDF Result Registers. When timer value exceeds selected register compared data, an internal event is generated.
Each channel creates 5 internal events. The LUT dictates the sequence of the PSG Output, the operation of the counters and the timing of hold command to T&H analog input units. One row (address) in the LUT dictates one state of the output sequence. LUT row contains 18 bits for determining the cycle structure as described in the following implementation example. Refer to Figure 2 and Figure 5.

Each PSG Channel includes:

Pulse by Pulse width limit driven by selected external events,
Shutdown mechanism driven by Over/Under limits of selected inputs and/or predefined external events with shutdown delay after a configurable number of PSG cycles.

Lighting and Building Control Applications

The IDC2000 is a powerful digital SoC controller for lighting and building control that integrates all the functions of a high performance networkable electronic ballast into one single chip. This controller comprises all the control and protection functions of the ballast and lamps including an embedded power line carrier modem. Additional optional communication interfaces provided by the IDC2000 are: microLan, RS485, I^2C, DC control, etc. for wired remote control and local control like RF (radio frequency) and IR (infrared). It also provides interfaces for occupancy and lighting sensors, other digital and analog control I/Os. The configuration capability of this controller eliminates the need to tune the circuit by selection of passive components.

The ASIC also can be used to provide the functions required by the master and local remote controls in building control systems.

The IDC2000 provides solutions for electronic ballasts with major advantages:

Low Cost - Simplified power topologies, integration of the communication function in the ASIC controller and smart control algorithms, dramatically reduce component count, the need of component accuracy and material cost.

Time to Market - GUI design tools created for the IDC2000 configuration allow each customer to incorporate proprietary control algorithms, power topology and lamp type, adjusting and tuning the ballast in a few days, all w/o code programming.

Development Effort/Cost - Allows the designer to create a ballast with the highest performances and lamp life parameters at all light levels using a common ballast hardware platform.

Remote Control Options - Embedded Power Line Carrier Modem, RF interface and other standard (I2C) communication interfaces enabling many of the remote control options desired in the market.

Common Hardware Platform - The IDC2000 does all the performance variations by means of programming the silicon logic using a GUI tool. No need of components to adjust and tune the ballast.

Available Design Tools – The PDK3 and demo board kits provide the designer easy to follow and rapid support to working ballast systems that meet their companies unique specifications.

Individual Lamp Protection Individual, separate control, command and protection of each lamp or group of lamps in a light fixture.

Flexible Lamp Control - Allows the implementation of a ballast driving a multiplicity of lamps working in parallel, each one individually controlled and protected. Different types of lamps working in parallel at their best operating conditions and controlled by the same controller.

Multi-Fixture Ballast - Provides a low cost, high performance multi-fixture (central) ballast, allowing each fixture to use a different type of lamp with separate control for dimming, shutdown and protection and providing equal light levels for fixtures installed at different distances.

Emergency Operation - Combine common ballast operation with emergency function with smart battery management.

Energy Savings – IDC2000 allows excellent BEF at low light levels. Separate lamp control allows further savings by individual shutdown of lamps instead of using dimming. Network Systems features can be added by easily connecting occupancy and analog light sensors, etc. directly to the IDC2000.

Load Shedding - Allows load shedding by dimming or shutting down individual lamps in each fixture.

Power Factor Correction - Embedded digital PFC configurable to the most advantageous power topology and operation mode - continuous, discontinuous and critical or a combination – thereof enabling lower THD at every light level.

Control Options – Allows selection from a library of different methods of dimming: PWM, FM, Phase Control, etc. or a combination thereof – or the customization of the designer's proprietary solution.

Application example for 1, 2 and 3xCFL26W ballast

The following table comprises test results of a low cost (~$10 components), high performance and fully featured networkable 3 lamps individually-operated ballast reference design, controlled with the IDC2000 emulator. This reference design has PLC communication interface in compliance with FCC and CENELEC standards

Notes: 1- All the measurements in the following table are carried out under 120VAC input

2- Stand-by power consumption: 0.5W including the power line receiver under operation

Table of Electrical Characteristics

Light level [%]		105	64	30	10	2
DC Bus [V]		367	223	212	212	234
Input Power [W] *	3 lamps	88.2	50.6	32.5	21.3	17.6
	2 lamps	60.0	34.4	22.0	14.5	12.0
	1 lamp	31.8	20.3	13.4	9.1	7.7
PF		0.99	0.99	0.99	0.99	0.98
THD [%] (3 lamps)		1.70	2.10	2.60	5.90	6.80
Lamp Voltage [V]		81.3	123	147	159	163
Lamp Current [mA]		303	108	44	16	7.5
Peak current [mA]		960	305	125	48	21
Lamp Current CF **		1.56	1.41	1.42	1.50	1.40
Filament [V]		1.40	1.92	2.70	3.00	3.40
Light level LF ripple (mV RMS)		26	4	7	3	2.7
Flicker [%]		0.5	0.1	0.5	0.6	2.3
BEF Ballast Efficacy Factor	3 lamps	1.19	1.27	0.92	0.47	0.11
	2 lamps	1.75	1.86	1.36	0.69	0.17
	1 lamp	3.30	3.15	2.24	1.09	0.26

The following functions, algorithms and topologies can be mainly substantiated with the IDC2000 and are part of the differentiators between the IDC2000 and existing controller available in the market for regular electronic ballasts and networkable electronic ballast in particular.

Programmed Start Up

Note: The following start up procedure is an example of what can be achieved by taking advantage of the IDC2000 capability to create different sequences of regimes. Each regime comprises its own pulse width and sequence variations. Each regime is applied at the corresponding ballast operation stage, thus allowing the designer to create any desired control algorithm.

- Soft start of the Preheat stage in order to prevent a flash at start-up by gradually increasing the HSD (high side switch) pulse width until reaching the desired pulse width which provides appropriate preheat at minimal lamp voltage. This procedure eliminates the lamp glow current during preheat. This pulse width is a pre-programmed parameter set during the ballast design.
- At the end of preheat prepare for ignition by reducing to minimum LSD (low side switch) pulse width and gradually increasing the HSD pulse width to the Ignition Value as pre-programmed parameter set during the ballast design. This procedure prevents spontaneous ignition.
- Ignite the lamp to the Ignition Light Level (pre-programmed function parameter set during ballast design) by closing the control loop on corresponding lamp current. This procedure provides controlled reliable ignition.
- On-the-fly change of control function parameters from Ignition to the lamp operation mode.
- The above program start up is implemented without the need of any passive components.
- An example of achievable (measured) start-up parameters:

Parameter	Preheat voltage	Glow current at preheat	Ignition voltage
Value	55Vrms	<1.5mArms	330Vrms 975Vpp

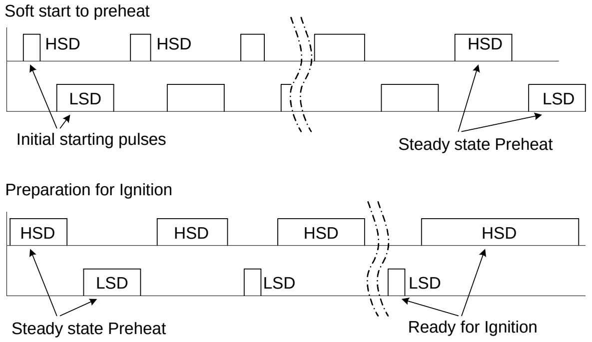


Figure 2. Start-Up Drive examples

Ignition procedure

Ignition can be carried out in different modes. One mode, shown in fig. 3, is: first igniting the lamp to the Ignition Light Level (a parameter fixed during the ballast design stage) and then changing to the Last Light Level. If Last Light Level is higher than the Ignition Light Level the light will continue to climb to it at the programmed fading rate. If the Last Light Level is lower than the Ignition Light Level then the light will dim down to the Last Light Level after the Ignition Light Level Hold Time. This ensures reliable ignition to very low light levels.

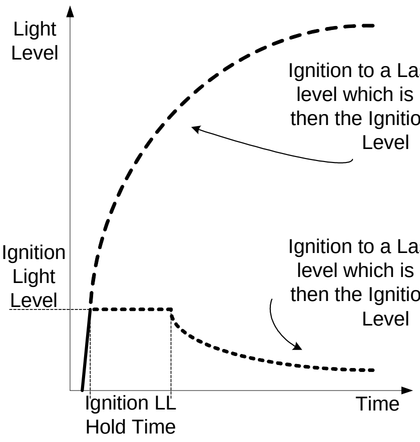


Fig. 3 Ignition Procedure example

Light Level Dependent Parameters [HSD, DC-Bus, THD (total harmonic distortion), Gains] – Example

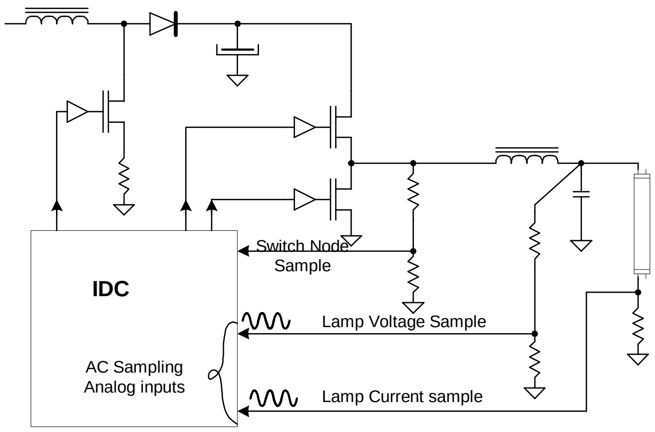
A look up table shown below inserts different sets of parameters for 32 light levels.

Bit #	0	1	2	…	29	30	31
Light Level (%)	1	2	4	…	86	100	115
Lamp current (mV)	6	14	27	…	780	1150	1500
HSD (uSec)	13	13	13	…	12	11.5	11
C Bus (V)	230	230	230	…	240	250	250
PFC (power factor correction) On threshold current (mV)	280	280	280	…	190	180	180

Parameters at every light level for: best efficiency, stabile light, required filament voltage and lowest THD

Note: The values in the Light Level and the Lamp current rows are obtained automatically from the lamp data base as created by the designer as mentioned below.

Using Lamp Current and Voltage AC Signals for control and protection functions (no need for rectification)



Lamp Instant Current and Lamp Instant Voltage are monitored several times at every HF (high frequency) cycle. This feature can provide the following benefits:

•Higher signal bandwidth •DC information •Lower component count •Flexible digital filtering •Every lamp of the system is monitored and controlled independently •Fast protection, HV (high voltage) event is detected within the first cycle of occurrence

Dynamic dead time by sensing the half bridge switch node and applying it as an event to enable driving of half bridge switches (switch node protection)

•Zero voltage switching •Half bridge load kept inductive •No cross conduction currents •Dead time interval minimized – maximizing the throughput power

The IDC enables the use of many power topologies and many control algorithms in order to create the best required ballast.

Fig. 4 depicts a ballast example using a novel economical half bridge power topology:

- One high side switch, three (>1) low side switches
- Every lamp is monitored and controlled separately
- Individual ON/OFF command is possible for every lamp
- Each lamp is protected individually – its circuit shuts down at lamp EOL (end of life)

Pulse trains for two light level regimes are displayed in fig. 5. These pulse trains belong to the above ballast topology and demonstrate the IDC2000 capabilities

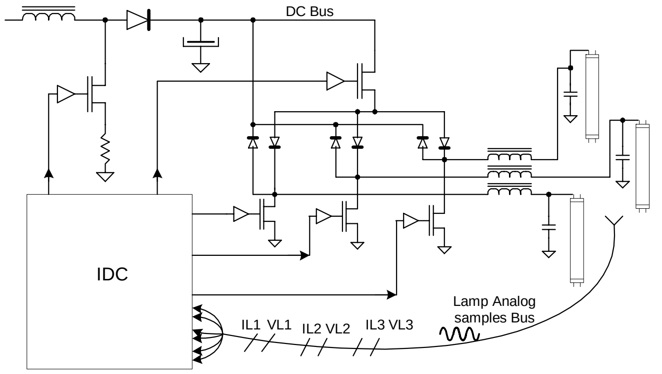


Fig. 4 Economic Common HS Topology - example

HSD & LSD pulses for light level regime A:

- Open loop fixed selected HSD interval
- Dynamic dead time before activating the low sides
- Light control performed by LSD pulse width for each lamp
- Fixed K interval for low side control
- All three LSDs start together

HSD & LSD pulses for light level regime B:

- Open loop fixed selected HSD interval
- Light control performed by LSD pulse width for each lamp
- Dynamic dead time from LSD to HSD and vice versa
- Dynamic dead time from LSD to HSD starts after end of the longest LSD interval
- L1 L2 L3 intervals of regime B are dynamically created and may vary from cycle to cycle

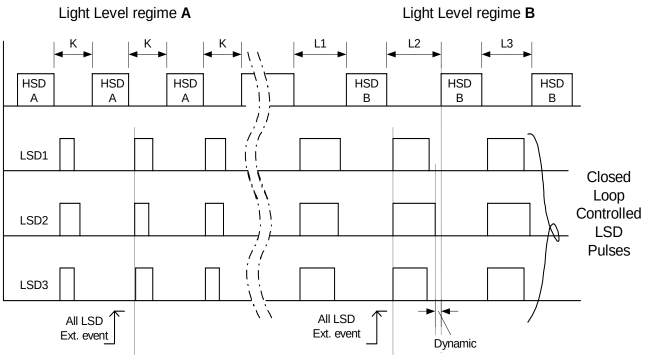
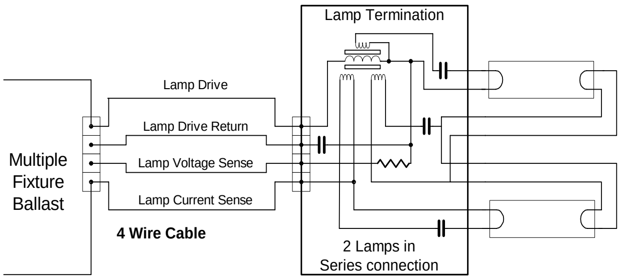


Figure 5 PSG Pulse Sequence Structure – example

Central ballast capabilities
The IDC2000 is a multi channel control device. It has a configured number of output drives and analog inputs. This enables driving multiple light channels while controlling each one of them separately with individual voltage and current feedback per channel as depicted in figure below.
Lamps are independently controlled and protected no matter which power topology is used nor the distance from the ballast to the lamp fixture.

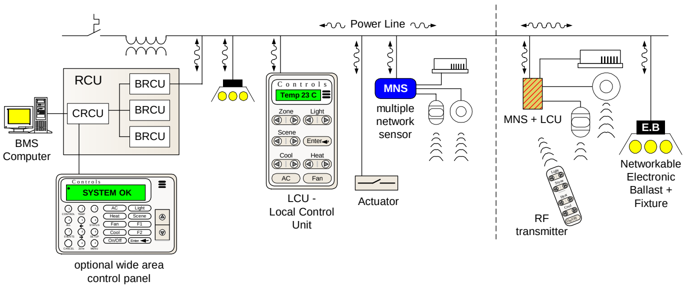


Using the above novel power topology for a central ballast, all lamps are controlled independently to one desired light level, each channel can be activated and deactivated separately, and in the case of local failure, only the bad lamp will turn off.

The IDC can also be configured to drive a configured number of totally independent half-bridges, where every light fixture may use a different lamp type and be controlled to a different light level.

Communication Command and Control

- Inherent power line carrier communication which was designed for lighting and HVAC networking and provides all the functionality of the DALI and more at a small fraction of market solutions cost, using inherent resources of the chip.
- Communicates bi-directionally 2 Kbits/sec rate over the power line having high reliability with a bit error rate less than 10^{-10} for a signal to noise ration of 8dB. Allows lighting commands, monitoring ballast & lamp status and sensors.
- Capability to individually control and monitor for EOL of every single lamp of a lighting system – muli-lamp or multi-fixture ballast.
- Built-in additional communication interfaces: 2.4GHz RF, 2 x UART full duplex up to 1.5 Mbit/sec
- IDC is the heart of remote controls: having PLC modem & many digital I/Os & analog inputs.



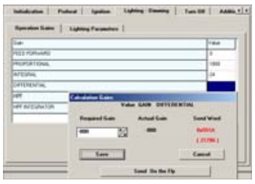
Configuration Design Tools

IDC architecture inherently allows the designer to create his ASIC by configuring this architecture using the following design tools without the arduous design process and without need to fabricate his own silicon.

PowerScene™ a GUI based high level automatic S/W tool used during the development stage enables the designer to configure the IDC2000 architecture using engineering constants (fixed control parameters) to adapt the controller to the targeted power topology, define the algorithms required by the application.

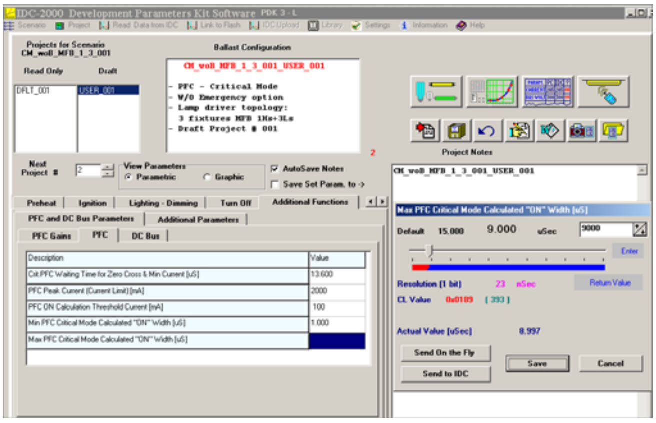
The PDK™, a GUI design tool allows the designer to develop a new light application with the following capabilities:

- Set ballast configuration by selecting the desired power topology and control algorithms from a library
- Insert ballast parameters set and create (or choose from library) lamps data base using the PDK tool.
- Modify parameters to obtain best ballast performance
- Modify a large portion of the parameters on-the-fly while the ballast is operating and lamps are lit to obtain the desired performance in a matter of minutes in a fully protected environment.
- The ability to re-configure the ballast and to change all design parameters enables less hardware models, no hardware trimming, and fast new model design.
- Modify selected parameters remotely over the power line using PLC



Gains Programming Ballast operational gains can be changed under operation for best stability

Lamp Light Curve -Normalizing a particular lamp current feedback signal to lamp light level in order to use it to control lamp light



Projects for Scenario CM_woB_MFB_1_3_001

Read Only: DFLT_001

Draft: USER_001

Ballast Configuration

CM_woB_MFB_1_3_001_USER_001
- PFC - Critical Mode
- W/O Emergency option
- Lamp driver topology:
  3 fixtures MFB 1Hs+3Ls
- Draft Project # 001

Next Project # 2

View Parameters: ● Parametric ○ Graphic

☑ AutoSave Notes

☐ Save Set Param. to ->

CM_woB_MFB_1_3_001_USER_001

Description	Value
Crit.PFC Waiting Time for Zero Cross & Min Current [uS]	13.600
PFC Peak Current (Current Limit) [mA]	2000
PFC ON Calculation Threshold Current [mA]	100
Min PFC Critical Mode Calculated "ON" Width [uS]	1.000
Max PFC Critical Mode Calculated "ON" Width [uS]	

Max PFC Critical Mode Calculated "ON" Width [uS]

Default 15.000 9.000 uSec 9000

Resolution (1 bit) 23 nSec

CL Value 0x0189 (393)

Actual Value [uSec] 8.997

PFC Programming - PFC parameters can be changed under operation (on the fly) for lowest THD